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Docket No.: 60188-126

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of : Customer Number: 20277  
Junichi YANO, et al. : Confirmation Number: 1397  
Serial No.: 10/001,967 ✓ : Group Art Unit: 2111  
Filed: December 05, 2001 : Examiner: Kim, Kenneth S.  
For: INTEGRATED CIRCUIT WITH CPU AND FPGA FOR RESERVED  
INSTRUCTIONS EXECUTION WITH CONFIGURATION DIAGNOSIS (As  
Amended)

**INFORMATION DISCLOSURE STATEMENT**

Mail Stop. ISSUE FEE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee.

**REQUEST TO CONSIDER REFERENCES AFTER CLOSE OF PROSECUTION AND  
BEFORE PAYMENT OF ISSUE FEE**

The undersigned hereby requests consideration and entry of this Information Disclosure Statement and accompanying references under 37 CFR 1.97(d).

Please charge the processing fee under 1.17(p) of \$180.00 to Deposit Account 500417.

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**CERTIFICATION PARAGRAPH**

The undersigned certifies that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement as described in 37 CFR 1.97(e)(1).

Each non-English language reference, listed on the attached PTO-1449, have been cited in a corresponding Japanese application office action and its relevance discussed therein. A copy of the foreign office action, together with an English language version thereof, is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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